generate the circuit and place it in the schematic. Since these cells are hierarchical, the primitive devices and auto-wiring are placed by creating an instance of the schematic p-cell and then flattening the element.

To maintain the hierarchy during the layout phase of the design, an instance box is placed in the schematic retaining the input parameters and device names and characteristics as properties and the elements are recognized and the primitives are replaced with the hierarchical p-cell.

To produce multiple implementations using different inherited parameter variable inputs, different embodiments of the same circuit type may be created by the methodology of the invention. In this process, the schematic is renamed to be able to produce multiple implementations in a common chip or design; the renaming process allows for the design system to distinguish multiple cell views to be present in a common design.

When the inherited parameters are defined, the circuit schematic is generated according to the selected variables. For example, substrate, ground and pin connections are established for the system to identify the connectivity of the circuit.

The design system may additionally auto-generate the layout from the electrical schematic which will appear as equivalent to the previously discussed graphical implementation.

The physical layout of the resistors circuits is implemented with p-cells using existing primitives in the reference library. The circuit topology is formed within the p-cell including wiring such that all parasitics may be accounted for.

It should be understood that the design system and methodology permits for change of circuit topology as well as structure size of the resistor structure in an automated fashion. Layout and circuit schematics are auto-generated with the user varying the number of elements in the circuit. The circuit topology automation allows for the customer to auto-generate new resistor elements without additional design work. Interconnects and wiring to and between the resistor elements are also auto-generated.

The resistor elements described herein with respect to FIGS. **1** and **2** and embodied as a hierarchical parameterized cell designed via the CAD tool kit of the invention, may thus be designed with the following achievable design objectives including, but not limited to: 1) verification of the connection between a first and second element by verifying and checking electrical connectivity wherein the first element is a p-cell and the second element is a p-cell; 2) verification of the width requirements to maintain high current and ESD robustness to a minimum level; 3) verify that based on the high current or ESD robustness of the ESD network that the resistor width and via number is such to avoid electrical interconnect failure prior to the ESD network failure; 4) allow for parallel resistors whose cross section can be maintained and evaluated as a set of parallel resistors; 5) allow for "resistor ballasting" by dividing into a plurality or array of resistors; 6) allow for calculation of the high current robustness of the resistor based on pulse width, surrounding insulator materials (e.g. SiO-.sub.2 or low K materials), metal level and distance from the substrate (thermal resistance based on the metal level or underlying structures; 7) account for surrounding fill shapes around the resistor p-cell; and, 8) account and adjust for "cheesing" (removal of interconnect material inside the interconnect) of the resistor element.

Various modifications may be made to the structures of the invention as set forth above without departing from the spirit and scope of the invention as described and claimed. Various aspects of the embodiments described above may be combined and/or modified.

While the invention has been particularly shown and described with respect to illustrative and preferred embodiments thereof, it will be understood by those skilled in the art that the foregoing and other changes in form and details may be made therein without departing from the spirit and scope of the invention that should be limited only by the scope of the appended claims.

The invention claimed is:

1. A computer-aided design system comprising:

means for generating two or more parameterized cell (P-cell) data structures representing two or more semiconductor film elements, each film element of a material type and thickness having desired properties in association therewith; and,

means for combining said two or more P-cells to automatically generate a higher order p-cell data structure representing a semiconductor resistor device having desired one or more properties tailored according to inherited properties of the semiconductor film element p-cells utilized in said combination, said semiconductor resistor device comprising a composite film of alternating layers of insulative and conductive material films designed to have a desired resistance value and optimized Temperature Coefficient of Resistance (TCR) value.

2. The computer-aided design system as claimed in claim **1**, wherein a tailored semiconductor device includes a resistor element having one or more desired properties including one or more of: an ESD value; a degree of lateral and vertical resistor self-ballasting.

3. The computer-aided design system as claimed in claim **1**, wherein said means for generating a parameterized cell (P-cell) data structure includes a graphical layout generator including an interface means enabling a graphical layout cell view of said resistor element, said interface means enabling user specification of parameters to be used in the generation of a P-cell data structure or higher order p-cell data structure representing said resistor element.

4. The computer-aided design system as claimed in claim **1**, wherein said means for generating a parameterized cell (P-cell) data structure includes a schematic layout generator including an interface means enabling a schematic cell view of said resistor element, said interface means enabling user specification of parameters to be used in the generation of a P-cell data structure or higher order p-cell data structure representing said resistor element.

5. The computer-aided design system as claimed in claim **3**, further including means enabling autogeneration of a circuit utilizing p-cell or higher order p-cell data structures to be included in said circuit for enabling the tailoring of circuit performance according to user specification.

6. A computer-implemented method of computer-aided design comprising the steps of:

a) generating, by a computer, two or more parameterized cell (P-cell) data structures representing two or more semiconductor film elements, each film element of a material type and thickness having desired properties in association therewith; and,

b) automatically generating, by a computer, a higher order p-cell data structure by combining said two or more p-cells, said higher order p-cell data structure representing a semiconductor resistor device having desired one or more properties tailored according to properties inherited from the semiconductor film element p-cells utilized in said combination, said semiconductor resistor device comprising a composite film of alternating layers of insulative and conductive material films designed to have a desired resistance value and optimized Temperature Coefficient of Resistance (TCR) value.

* * * * *